AMENDMENT TO THE CLAIMS

Claims 1-3 (Canceled)

Claim 4. (Currently Amended) A test method for a semiconductor device in which a bonding pad thereof comprises a first interconnect layer and a second interconnect layer, said bonding pad comprising;:

a plurality of slit-shaped trenches arranged parallel to each other and formed within an interlayer insulation film provided between said first and second interconnect layers,

a first connection part provided within one of said slit-shaped trenches and connecting said first interconnect layer and said second interconnect layer,

a second connection part and a third connection part provided within other slit-shaped trenches and connecting said first interconnect layer and said second interconnect layer, respectively, said second connection part and said third connection part being disposed so as to sandwich said first connection part with a prescribed spacing,

a first bridge connecting part and a second bridge connecting part, formed in said interlayer insulation film, connecting said first connection part and said second connection part, and

a third bridge connecting part, formed in said interlayer insulation film, connecting said first connection part and said third connection part, said third bridge connecting part being disposed between said first bridge connecting part and said second bridge connecting part,

wherein said method comprising; contacting a test probe for testing said semiconductor device with said bonding pads so as to be in a direction parallel to a longitudinal direction of said connection part.

Claim 5. (Currently Amended) A test method for a semiconductor device in which a bonding pad thereof comprises a first interconnect layer and a second interconnect layer, said bonding pad comprising:

a plurality of connection parts, provided within a plurality of slit-shaped trenches formed in an interlayer insulation film, respectively, and connecting said first interconnect layer and said second interconnect layer, said connection parts being disposed in one direction with a prescribed spacing,

wherein said method comprising;- contacting a test probe for testing said semiconductor device with said bonding pads so as to be in a direction parallel to a longitudinal direction of said connection part.

6. (New) The semiconductor device according to claim 4, wherein said first connection part is disposed in a longitudinal direction parallel to an insertion direction of said test probe during a chip test.

7. (New) The semiconductor device according to claim 5, wherein said first connection part is disposed in a longitudinal direction parallel to an insertion direction of said test probe during a chip test.

8. (New) The semiconductor device according to claim 4, wherein said second interconnect layer has a thickness in a range from 0.9 - 1.7 μm.

9. (New) The semiconductor device according to claim 5, wherein said second interconnect layer has a thickness in a range from 0.9 - 1.7 μm.

10. (New) The semiconductor device according to claim 4, wherein an insertion direction of said test probe is perpendicular to a boundary between said first connection part and said interlayer insulation film.

11. (New) A test method for a semiconductor device in which a bonding pad thereof comprises a first interconnect layer and a second interconnect layer, said bonding pad comprising:

a plurality of slit-shaped trenches arranged parallel to each other and formed within an interlayer insulation film provided between said first interconnect layer and said second interconnect layer; and

a connection part provided within one of said plurality of slit-shaped trenches and connecting said first interconnect layer and said second interconnect layer,

wherein said method comprising contacting a test probe for testing said semiconductor device with said bonding pad so as to be in a direction parallel to a longitudinal direction of said connection part.